

PCI bus bridge for MC680x0 based computer system using PLD technology

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ABSTRACT

Peripheral Connect Interface (PCI) is a well established industry standard bus used for connecting CPU to peripheral devices. PCI gives access to many good quality and inexpensive peripherals. There are plenty of PCI host bridge chips for commonly used CPUs like x86 compatible or PowerPC. It is sometimes necessary to interface PCI device with an older or specific computer systems based on other processors, to expand their capabilities. If dedicated bridge chip is not available (or even do not exists) the bus can be interfaced via PLD integrated circuits. The paper describes add-on PCI bridgeboard for Amiga 4000 computer (based on Motorola MC68060 CPU), designed with Altera MAX7000 PLD chips.

Keywords: PCI bridge, Motorola MC680x0, PLD devices, MAX 7000.

1. INTRODUCTION

The PCI bridgeboard was designed to allow using inexpensive PCI graphics, Ethernet and other cards in an Amiga 4000 computer. This computer system has a custom expansion bus codenamed *Zorro III*. It is 32-bit asynchronous, data/address multiplexed bus, based roughly on Motorola MC68030 system bus. The bridgeboard has been designed for four PCI cards. It occupies 512 MB of CPU address space divided into four address ranges given in the Table 1.

Tab. 1. Bridgeboard address space.

Address	Description
Base + \$00000000 to Base + \$0000FFFF	PC legacy I/O space
Base + \$00010000 to Base + \$000EFFFF	PCI I/O space
Base + \$000F0000 to Base + \$000FFFFFFF	PCI configuration space
Base + \$00100000 to Base + \$1FFFFFFF	PCI memory space

Base address is assigned to the board by operating system during boot. The bridge provides 960 kB of PCI I/O space and 511 MB of PCI memory space. It is enough for typical, four cards setup (for example graphics, Ethernet, sound and USB controller). In contrast to standard PC architecture, configuration spaces for every PCI slot are memory-mapped (PC uses access through two longword registers). Such an approach significantly simplifies address decoder design.

Two EPM7128SQC160-15 (Altera) PLD devices was chosen to implement the bridge core, for their availability and low cost of components and programming device. The design requires a

high number of pins, while the logic is relatively simple. That is why two 160-pin PLD devices have been used instead of one 208-pin with doubled logic capacity. Altera as well as other PLD vendors provides ready PCI megafunctions, but these require much more expensive devices (like FLEX10k) and are commercial products. That is why the bridge has to be designed from scratch. The first chip contains control section with state machines for the two bridged buses, the second one contains the multiplexed address/data path of the bridge and address decoders. Bridge functions have been distributed between the two chips in a way minimizing the number of connections between them.

2. BRIDGE DESIGN

Described bridge is somewhat limited PCI 2.1 implementation, because it can only act as a PCI master device. It can however grant the bus to any PCI device installed, for performing DMA data transfer between two PCI devices. DMA between PCI device and the host memory is not possible, it can be emulated using graphics board video memory as a temporary buffer. As Zorro III is a multiplexed bus, the address of transaction have to be latched in the Zorro III address latch. Basing on the latched address, Zorro III address decoder checks if bus operation is addressed to the bridge. Zorro state machine is signalled if decoding result is positive. Then the cycle begins. The bus is asynchronous, so Zorro III

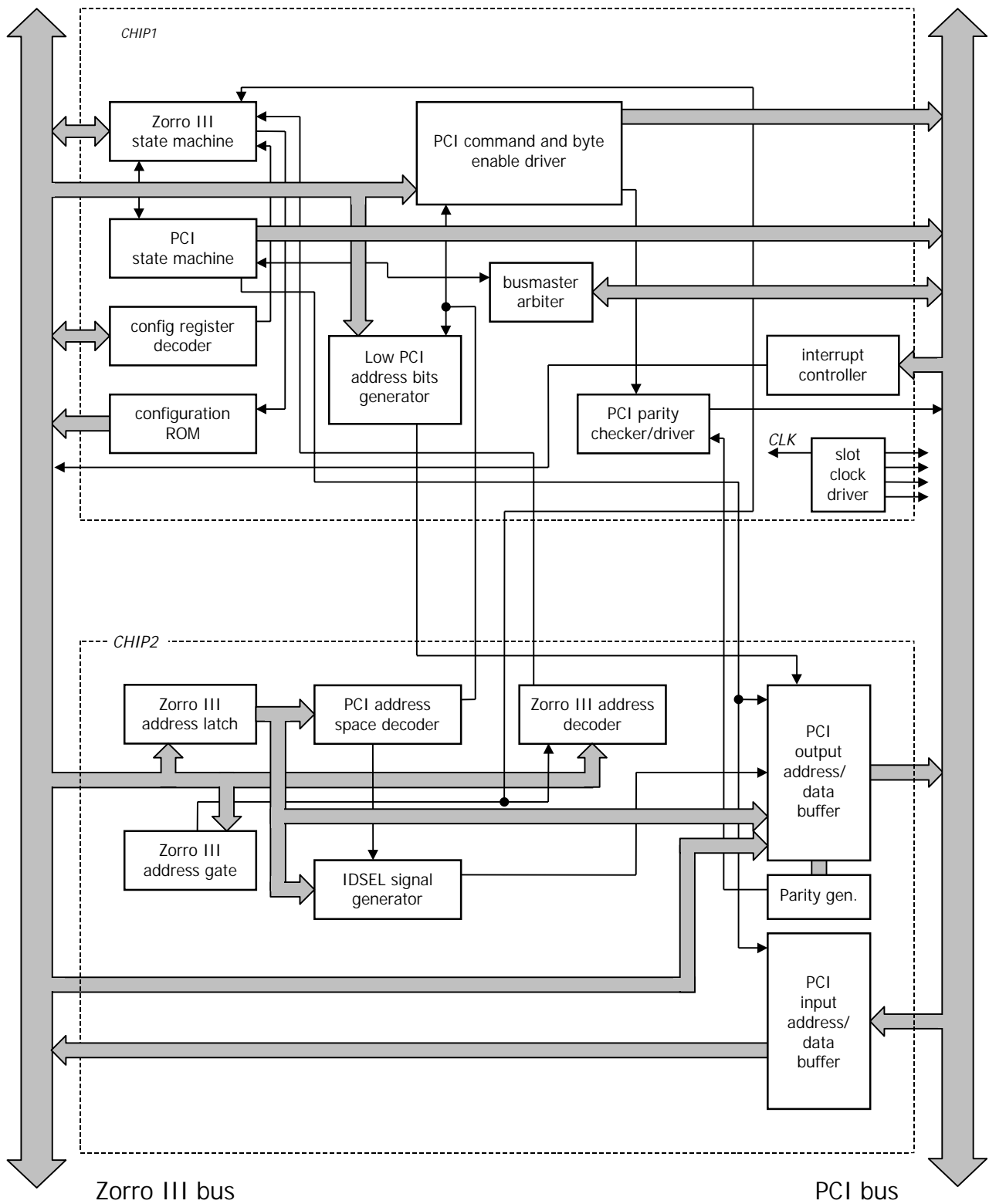


Fig. 1. PCI bridge functional diagram.

state machine is really a combinatorial logic driven by Zorro III signals and PCI state machine. Zorro III state machine is also responsible for handling configuration register of the bridge and configuration ROM, these are used at boot time for bridge autoconfiguration. The main control block of the bridge is the PCI state machine. PCI bus operation is triggered by Zorro III logic, then PCI state machine takes control over the bridge operation. It drives and monitors important PCI control signals: FRAME, IRDY, TDRY, DEVSEL, STOP. PCI state machine supports master and target generated abort events. It also generates signals controlling PCI input and output registers, multiplexers and tri-state buffers placed in chip 2. The PCI parity generator calculates parity bit across AD[31:0] and C/BE[3:0] PCI lines. The bridge always generates, but not checks the parity bit. Busmaster arbiter is responsible for fair dividing the bus time between requesting devices. Busmaster time quantum has been set to 64 PCI clock cycles (2.112 μ s). If a PCI master device does not free the bus within the time quantum, it loses the bus ownership if any other PCI device wants to become a master. In the condition where all four devices are requesting bus grant, every one is given of bus time quantum in turn. PCI CB/E driver puts PCI command on C/BE[3:0] lines during PCI address phase, and byte enable signals during data phase. PCI command is derived from signals of Zorro III read/write signal and PCI address space decoder (PCI has separate commands for Memory, I/O and Configuration address spaces). Low PCI address bits generator is responsible for two lowest address bits (AD1 and AD0). These carry burst ordering information, or configuration cycle type (for configuration space accesses). The interrupt controller is a simple OR gate directing all four PCI interrupt lines to INT2 line of the host system. The clock driver generates five clock signals, one clocking both PLD devices, and four separate PCI slots clock, routed physically with separate tracks on PCB. Lengths of tracks are the same so PCI specification clock skew requirement can be met. The IDSEL signal generator is used during configuration cycles for selecting PCI device. While PCI device is unconfigured it has no valid base address, so it has to be addressed with IDSEL pin. IDSEL pins of four PCI slots have been routed to AD16 - AD19 lines as suggested in [1]. IDSEL generator drives logic "1" to one of these depending on access address within the memory mapped PCI configuration space of the bridge. The bridge has been physically designed as standard Zorro III expansion card. Four-layer printed circuit board has been used as recommended in [1]. All the components except PCI slots, quartz generator and power supply decoupling electrolytic capacitors are SMD devices. The bridge card is shown on Fig. 1. to Fig. 4. The gold-plated edge connector is Zorro III bus connector. The 4-pin high-current connector delivers +5 and +12 V power supply. All signals are routed on two external layers of PCB, two internal layers are ground and +5 V planes.

3. PICTURES OF THE BRIDGEBOARD

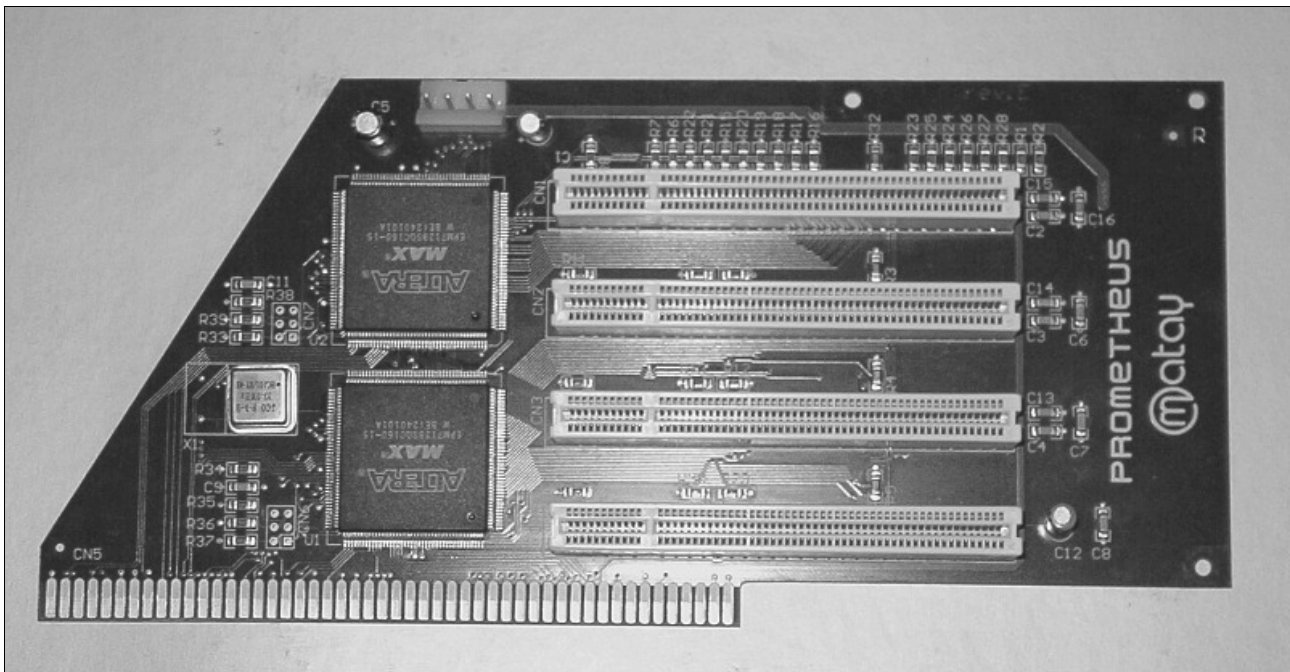


Fig. 2. Prototype PCI bridgeboard for MC680x0 system – top view.

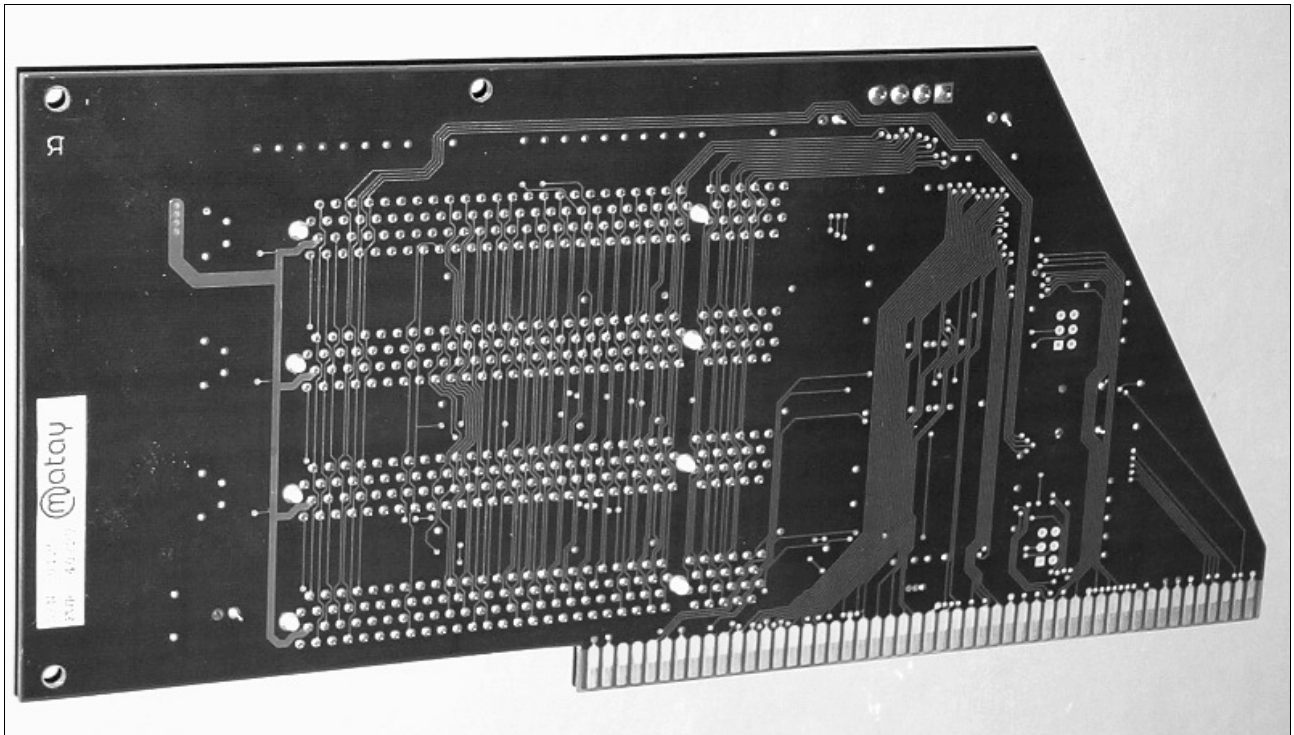


Fig. 3. Prototype PCI bridgeboard for MC680x0 based system – bottom view.

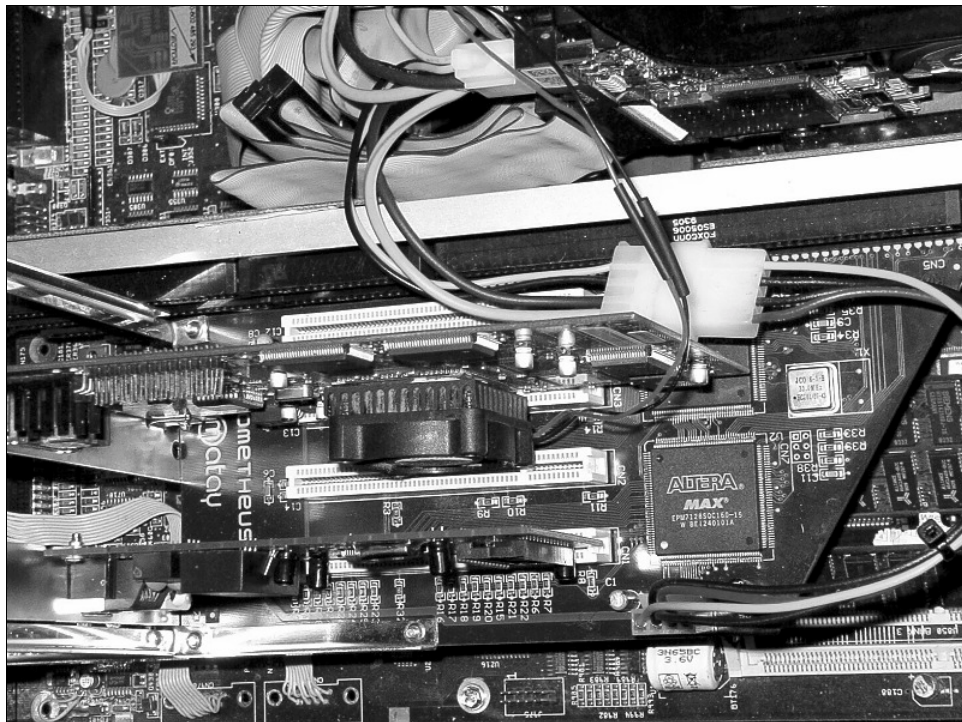


Fig. 4. Prototype PCI bridgeboard mounted in the system, equipped with Voodoo3 2000 graphics card and RTL8029 based Ethernet card.

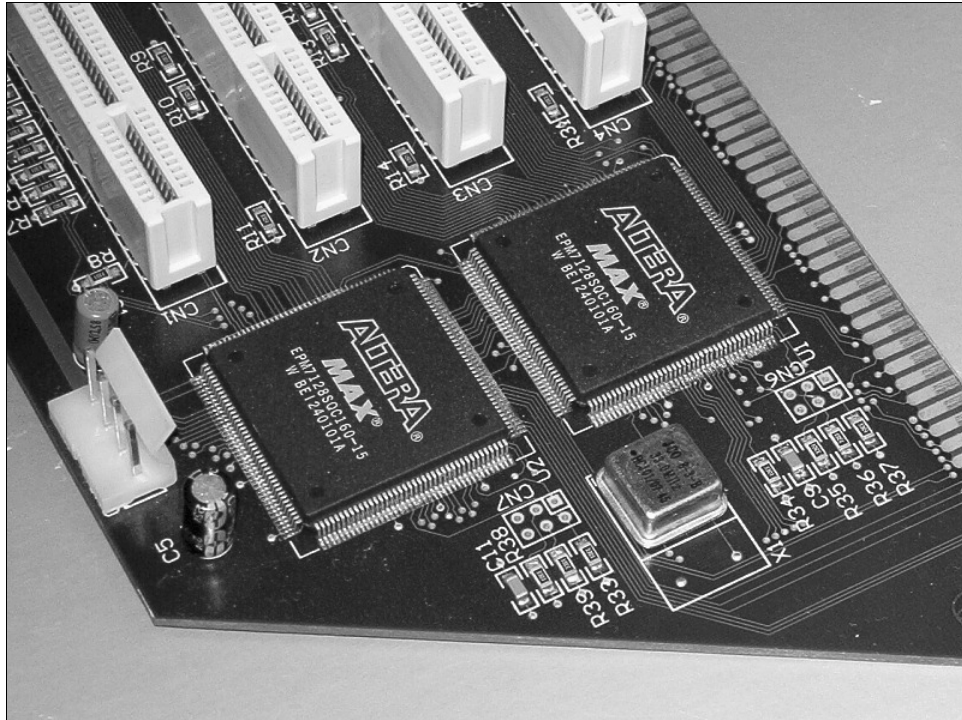


Fig. 5. The heart of the PCI bridge – Two PLD integrated circuits and 33 MHz quartz generator.

4. CONCLUSION

Described PCI bridge design for MC680x0 computer system proves that limited PCI implementations can be designed with relatively low capacity (and therefore low cost) PLD devices. 256 logic cells (every containing one flip-flop and combinatorial logic) were enough to implement full-featured PCI master device and host busmaster arbiter. Custom PCI bridge can be an optimal solution for low volume production of devices demanding high resolution graphics output, Ethernet connectivity or other functionality delivered by off-the-shelf PCI devices. The bridge has been produced in small series under *Prometheus* trade mark. There are drivers available for Voodoo3 graphics board (including 3D accelerator) and Ethernet boards based on RealTek RTL8029 chip.

REFERENCES

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2. *PCI Bus Applications*, application note AN41, Altera Corporation, 1995.
3. *MAX7000 Programmable Logic Device Family DataSheet*, Altera Corporation, 2002.